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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,327	02/12/2004	Nigel G. Herron	X-1545 US	4920

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EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,327	HERRON ET AL.	
	Examiner	Art Unit	
	David Ton	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☒ Claim(s) 28-30 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/12/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-30 are presented for examination.

Claim Rejections - 35 USC ' 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-3, 10-12, 14-15, 17-18, 20 and 22 are rejected under 35 U.S.C. § 102(e) as being anticipated by Shen et al. (Shen) patent no. 6,829,751.

4. As to claim 1, Shen teaches the invention as claimed, including a method for testing an integrated circuit [system on a chip, col. 1 lines 7-11] having an embedded

device [module 202a of Fig. 5] within a configurable logic fabric [FPGA core, col. 2 lines 39-55 5] comprising configuring the configurable logic fabric for a test comprising, forming a scan chain [SCAN_CHAIN_X of Fig. 3] in the configurable logic fabric [Fig. 3], providing scan data from at least a portion of the scan chain to the device and performing the test on the device [see col. 6 lines 45-56].

5. As to claims 2-3, Shen teaches the scan chain comprises a plurality of shift registers connect in series [REG 120a of fig. 2], plurality of logic block [PFGA core and logic 102 of Fig. 1].

6. As to claim 10, Shen teaches the invention as claimed including a method for testing an IC having configurable logic fabric and a fixed logic circuit comprising configuring the IC for test comprising forming a scan chain having test data. Furthermore, Shen teaches transferring the test data from the scan chain to a multiplexer [MUX 160 of Fig. 3], the multiplexer is a part of interfacing circuitry, the interfacing circuitry coupling the fixed logic circuit to the configurable logic fabric and transferring the test data from the multiplexer to the fixed logic circuit [col. 4 lines 12-23].

7. As to claim 11, Shen teaches the configuring the IC for test further comprises emulating test functions of an external tester [col. 4 lines 35-58].

8. As to claim 12, Shen teaches the fixed logic circuit is an embedded core device [module 202a of Fig. 5].

9. As to claim 14, Shen teaches a method for testing a PLD having an embedded fixed logic device comprising configuring the PLD for test by forming a scan chain as

shown in claim 1 above and also teaches sending an output test signal from the embedded fixed logic device to multiplexer [MUX 166b of Fig. 3] formed within a gasket [Fig. 3] and sending the output test signal from the multiplexer to the scan chain [scan_chain_x of Fig. 3].

10. As to claims 15 and 22, Shen teaches the PLD is FPGA [col. 1 lines 7-12].

11. As to claim 17, Shen teaches a system for testing a fixed logic circuit, comprising: a programmable logic fabric in an integrated circuit (IC) [see Fig. 5], wherein the fixed logic circuit [module 202a of Fig. 5] is embedded in the programmable logic fabric [FPGA core 116 of Fig. 5]; interconnecting logic, having a multiplexer [MUX 160 of Fig. 3], at least partially surrounding the fixed logic circuit, the interconnecting logic coupling the fixed logic circuit to the programmable logic fabric; and a scan chain formed in the programmable logic fabric for testing the fixed logic circuit via the multiplexer [col. 4 lines 12-23].

12. As to claims 18-20, Shen teaches a test analyzer formed in the programmable logic fabric [col. 1 lines 56-64], an external tester [debugging work station 104 of Fig. 3], and the scan chain is reconfigured to test the interconnecting logic [col. 1 lines 56-64].

Claim Rejections - 35 USC ' 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

> to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 4-9, 13, 16, 21, and 23-27 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Shen et al. (Shen) patent no. 6,829,751 in view of Whetsel patent no. 6,405,335.

15. As to claim 4, Shen teaches the invention as claimed, including the embedded device is a specific module [module 202a of Fig. 5]. However, Shen does not teach the module is a fixed logic core processor and the method further placing the fixed logic core processor in a predetermined state using the scan data.

Whetsel teaches a method of testing IC with scan paths and particularly, the IC having high complex embedded cores such as DSPs, CPUs, I/O peripherals, memories, and mixed signal A/D and D/A functions [see col. 1 lines 15-34 and claim 18] and the method further placing the fixed logic core processor in a predetermined state using the scan data [col. 42 lines 38-50].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to combine the teachings of Shen with the teachings of Whetsel by modifying the module testing taught by Shen for testing a core processor as taught by Whetsel. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide an application for Shen invention to test a highly complex property cores.

16. As to claim 5, Whetsel teaches another portion of the scan chain receiving test results from the embedded device [scan collector, see claim 1].

17. As to claim 6, Shen teaches transmitting the test results through the configurable logic fabric to an external tester for evaluation [debugging workstation 104 of Fig. 2].

18. As to claim 7, Whetsel teaches transmitting at least one test signal to a multiplexer for delivery to the embedded device [MUX 2402 of Fig. 24].

19. As to claim 8, Whetsel teaches receiving at least one test output signal from a multiplexer coupled to receive at least one output from the embedded device [MUX 2404 of Fig. 24].

20. As to claims 9, 16 and 21, Whetsel teaches the embedded device is selected from a group consisting of a digital signal processor, a microprocessor, a physical layer interface, a link layer interface, a network layer interface, an audio processor, a video graphics processor, a fixed logic circuit, and an application-specific integrated circuit [col. 1 lines 15-34].

21. As to claim 13, Whetsel teaches the embedded device is a processor [claim 18].

22. As to claim 23, Shen teaches test results produced from the fixed logic circuit [col. 2 lines 39-47].

23. As to claim 24, Whetsel teaches the interconnecting logic comprises on chip memory controller module and a controller [see Fig. 17].

24. As to claim 25-26, Whetsel teaches the scan chain comprises a latch shift register [see Fig. 21A-B].

25. As to claim 27, it is similar to claim 10; therefore, it is rejected under the same rationale.

Allowable Subject Matter

26. Claims 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

27. The prior art of record and not relied upon is considered pertinent to applicant's disclosure.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton whose telephone number is (571) 272-3828. The examiner can normally be reached on M-Th from 5:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Ton
Primary Examiner
Art Unit 2133